19-0229; Rev 7; 2/07

High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

General Description

The MAX941/MAX942/MAX944 are single/dual/quad high-speed comparators optimized for systems powered from a 3V or 5V supply. These devices combine high speed, low power, and rail-to-rail inputs. Propagation delay is 80ns, while supply current is only 350µA per comparator.

The input common-mode range of the MAX941/MAX942/MAX944 extends beyond both power-supply rails. The outputs pull to within 0.4V of either supply rail without external pullup circuitry, making these devices ideal for interface with both CMOS and TTL logic. All input and output pins can tolerate a continuous short-circuit fault condition to either rail.

Internal hysteresis ensures clean output switching, even with slow-moving input signals. The MAX941 features latch enable and device shutdown.

The single MAX941 and dual MAX942 are offered in a tiny µMAX® package. Both the single and dual MAX942 are available in 8-pin DIP and SO packages. The quad MAX944 comes in 14-pin DIP and narrow SO packages.

Applications

3V/5V Systems

Battery-Powered Systems

Threshold Detectors/Discriminators

Line Receivers

Zero-Crossing Detectors

Sampling Circuits

Features

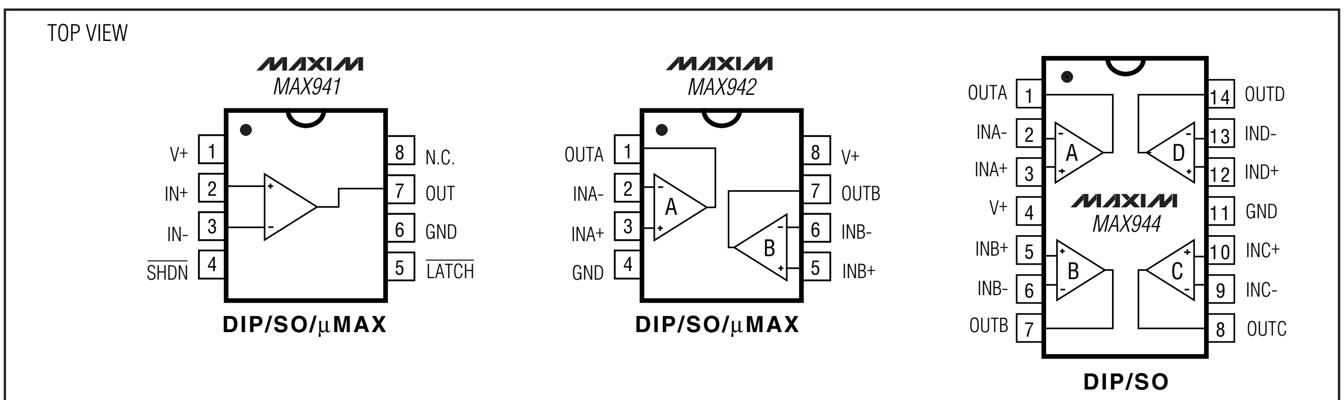
- ♦ **Available in µMAX Package for Automotive Applications**
- ♦ **Optimized for 3V and 5V Applications (Operation Down to 2.7V)**
- ♦ **Fast, 80ns Propagation Delay (5mV Overdrive)**
- ♦ **Rail-to-Rail Input Voltage Range**
- ♦ **Low 350µA Supply Current per Comparator**
- ♦ **Low, 1mV Offset Voltage**
- ♦ **Internal Hysteresis for Clean Switching**
- ♦ **Outputs Swing 200mV of Power Rails**
- ♦ **CMOS/TTL-Compatible Outputs**
- ♦ **Output Latch (MAX941 only)**
- ♦ **Shutdown Function (MAX941 only)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX941CPA	0°C to +70°C	8 Plastic DIP	P8-1
MAX941CSA	0°C to +70°C	8 SO	S8-2
MAX941EPA	-40°C to +85°C	8 Plastic DIP	P8-1
MAX941ESA	-40°C to +85°C	8 SO	S8-2
MAX941EUA-T	-40°C to +85°C	8 µMAX-8	U8-1
MAX941AUA-T	-40°C to +125°C	8 µMAX-8	U8-1

Ordering Information continued at end of data sheet.

Pin Configurations



High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

ABSOLUTE MAXIMUM RATINGS

Power-Supply Ranges
- Supply Voltage V+ to GND ....+6.5V
- Differential Input Voltage ....-0.3V to (V+ + 0.3V)
- Common-Mode Input Voltage ....-0.3V to (V+ + 0.3V)
- $\overline{\text{LATCH}}$ Input (MAX941 only) ....-0.3V to (V+ + 0.3V)
- $\overline{\text{SHDN}}$ Control Input (MAX941 only) ....-0.3V to (V+ + 0.3V)
- Current Into Input Pins...±20mA

Continuous Power Dissipation (T_A = +70°C)
- 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ...727mW
- 8-Pin SO (derate 5.88mW/°C above +70°C)................471mW
- 8-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW
- 14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)..800mW
- 14-Pin SO (derate 8.33mW/°C above +70°C).............667mW

Operating Temperature Ranges
- MAX94_C_ _ ....0°C to +70°C
- MAX94_E_ _..-40°C to +85°C
- MAX94_AUA ....-40°C to +125°C
- MAX942MSA...-55°C to +125°C

Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 2.7V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 14)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Positive Supply Voltage	V+				2.7		5.5	V
Input Voltage Range	V_{CMR}	(Note 1)			-0.2		V+ + 0.2	V
Input-Referred Trip Points	V_{TRIP}	V_{CM} = 0 or V_{CM} = V+ (Note 2)	T_A = +25°C	MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA		1	3	mV
				MAX941_UA/MAX942_UA		1	4	
			T_A = T_{MIN} to T_{MAX}	MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA			4	mV
				MAX941_UA/MAX942_UA			6	
Input Offset Voltage	V_{OS}	V_{CM} = 0 or V_{CM} = V+ (Note 3)	T_A = +25°C	MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA		1	2	mV
				MAX941_UA/MAX942_UA		1	3	
			T_A = T_{MIN} to T_{MAX}	MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA			3	mV
				MAX941_UA/MAX942_UA			5.5	
Input Bias Current	I_B	V_{IN} = V_{OS}, V_{CM} = 0 or V_{CM} = V+ (Note 4)		MAX94_C		150	300	nA
				MAX94_E/A, MAX942MSA		150	400	
Input Offset Current	I_{OS}	V_{IN} = V_{OS}, V_{CM} = 0 or V+				10	150	nA
Input Differential Clamp Voltage	V_{CLAMP}	Force 100µA into IN+, IN- = GND, measure V_{IN+} - V_{IN-}, Figure 3				2.2		V
Common-Mode Rejection Ratio	CMRR	(Note 5)		MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA		80	300	µV/V
				MAX941_UA/MAX942_UA		80	800	
Power-Supply Rejection Ratio	PSRR	2.7V ≤ V+ ≤ 5.5V, V_{CM} = 0V		MAX94_C_ _, MAX94_EP_, MAX94_ES_, MAX942MSA		80	300	µV/V
				MAX941_UA/MAX942_UA		80	350	
Output High Voltage	V_{OH}	I_{SOURCE} = 400µA			V+ - 0.4	V+ - 0.2		V
		I_{SOURCE} = 4mA			V+ - 0.4	V+ - 0.3		
Output Low Voltage	V_{OL}	I_{SINK} = 400µA				0.2	0.4	V
		I_{SINK} = 4mA				0.3	0.4	
Output Leakage Current	I_{LEAK}	(Note 6)					1	µA

ELECTRICAL CHARACTERISTICS (continued)

($V+ = 2.7V$ to $5.5V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at $T_A = +25°C$.) (Note 14)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current per Comparator	I_{CC}	V+ = 3V	MAX941		380	600	µA
			MAX942/MAX944		350	500	
		V+ = 5V	MAX941		430	700	
			MAX942/MAX944		400	600	
		MAX941 only, shutdown mode (V+ = 3V)			12	60	
Power Dissipation per Comparator	PD	(Note 7)	MAX941		1.0	4.2	mW
			MAX942/MAX944		1.0	3.6	
Propagation Delay	t_{PD+}, t_{PD-}	(Note 8)	MAX94_C		80	150	ns
			MAX94_E/A, MAX942MSA		80	200	
Differential Propagation Delay	dt_{PD}	(Note 9)			10		ns
Propagation Delay Skew		(Note 10)			10		ns
Logic Input Voltage High	V_{IH}	(Note 11)		$\frac{V+}{2} + 0.4$	$\frac{V+}{2}$		V
Logic Input Voltage Low	V_{IL}	(Note 11)			$\frac{V+}{2}$	$\frac{V+}{2} - 0.4$	V
Logic Input Current	I_{IL}, I_{IH}	V_{LOGIC} = 0 or V+ (Note 11)			2	10	µA
Data-to-Latch Setup Time	t_S	(Note 12)			20		ns
Latch-to-Data Hold Time	t_H	(Note 12)			30		ns
Latch Pulse Width	t_{LPW}	MAX941 only			50		ns
Latch Propagation Delay	t_{LPD}	MAX941 only			70		ns
Shutdown Time		(Note 13)			3		µs
Shutdown Disable Time		(Note 13)			10		µs

Note 1: Inferred from the CMRR test. Note also that either or both inputs can be driven to the absolute maximum limit (0.3V beyond either supply rail) without damage or false output inversion.

Note 2: The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone (see Figure 1).

Note 3: V_{OS} is defined as the center of the input-referred hysteresis zone (see Figure 1).

Note 4: The polarity of I_B reverses direction as V_{CM} approaches either supply rail. See *Typical Operating Characteristics* for more detail.

Note 5: Specified over the full common-mode range (V_{CMR}).

Note 6: Applies to the MAX941 only when in shutdown mode. Specification is for current flowing into or out of the output pin for V_{OUT} driven to any voltage from V+ to GND.

Note 7: Typical power dissipation specified with V+ = 3V; maximum with V+ = 5.5V.

Note 8: Parameter is guaranteed by design and specified with V_{OD} = 5mV and C_{LOAD} = 15pF in parallel with 400µA of sink or source current. V_{OS} is added to the overdrive voltage for low values of overdrive (see Figure 2).

Note 9: Specified between any two channels in the MAX942/MAX944.

Note 10: Specified as the difference between t_{PD+} and t_{PD-} for any one comparator.

Note 11: Applies to the MAX941 only for both $\overline{SHDN}$ and $\overline{LATCH}$ pins.

Note 12: Applies to the MAX941 only. Comparator is active with $\overline{LATCH}$ pin driven high and is latched with $\overline{LATCH}$ pin driven low (see Figure 2).

Note 13: Applicable to the MAX941 only. Comparator is active with $\overline{SHDN}$ pin driven high and is in shutdown with $\overline{SHDN}$ pin driven low. Shutdown disable time is the delay when $\overline{SHDN}$ is driven high to the time the output is valid.

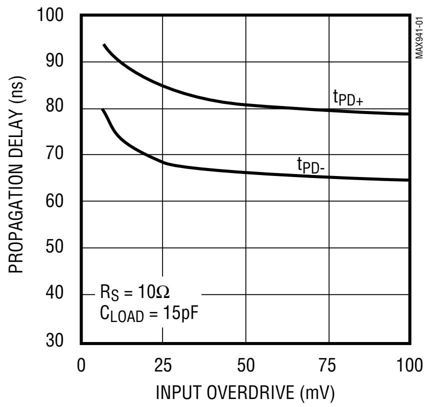
Note 14: The MAX941_UA and MAX942_UA are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

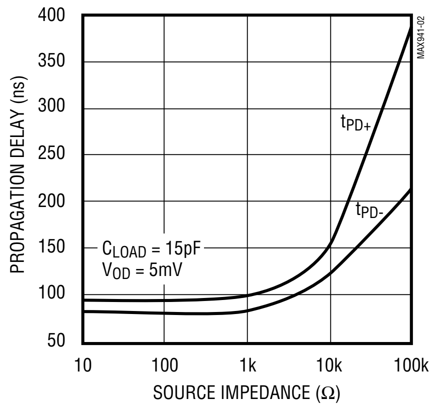
Typical Operating Characteristics

(V+ = 3.0V, T_A = +25°C, unless otherwise noted.)

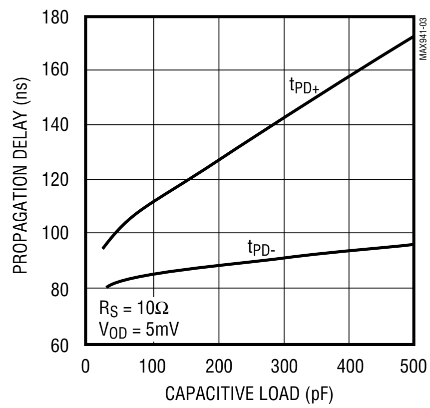
PROPAGATION DELAY vs. INPUT OVERDRIVE



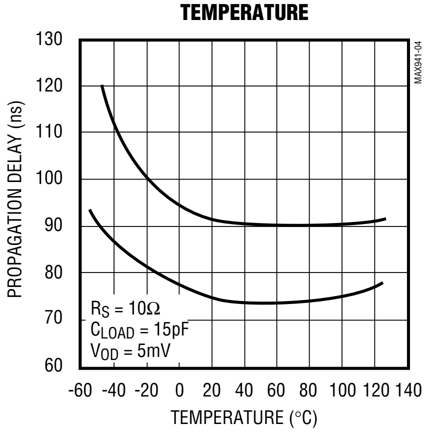
PROPAGATION DELAY vs. SOURCE IMPEDANCE



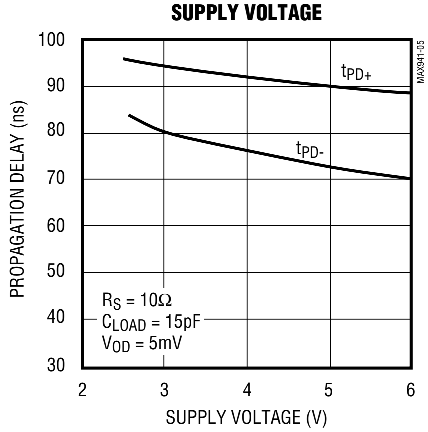
PROPAGATION DELAY vs. CAPACITIVE LOAD



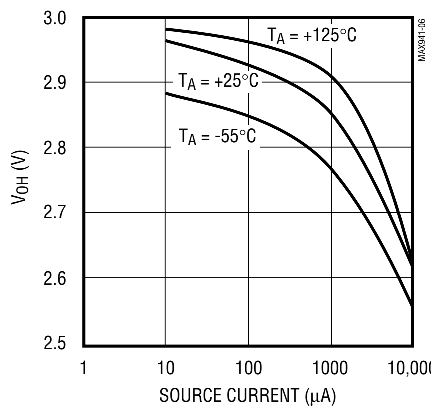
PROPAGATION DELAY vs. TEMPERATURE



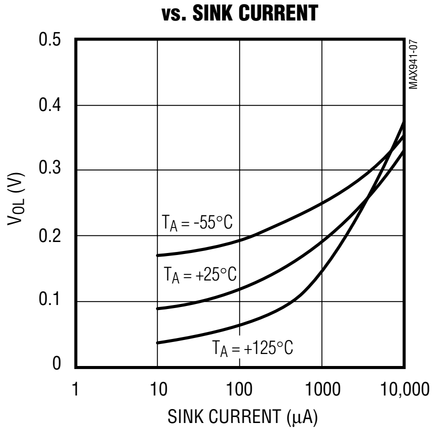
PROPAGATION DELAY vs. SUPPLY VOLTAGE



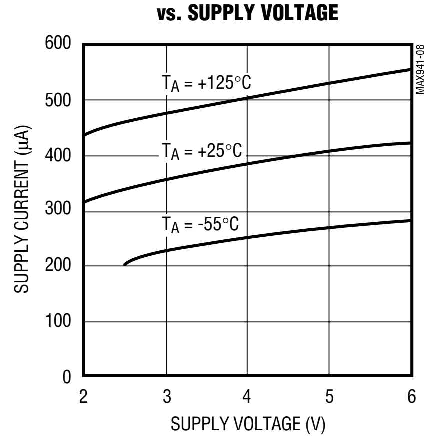
OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



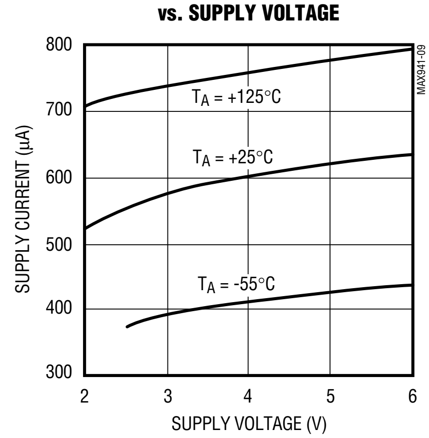
OUTPUT LOW VOLTAGE vs. SINK CURRENT



MAX941 TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



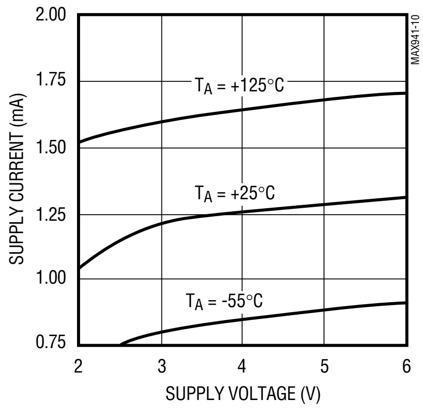
MAX942 TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



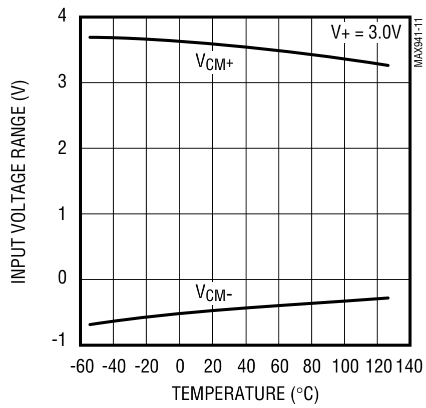
Typical Operating Characteristics (continued)

(V+ = 3.0V, T_A = +25°C, unless otherwise noted.)

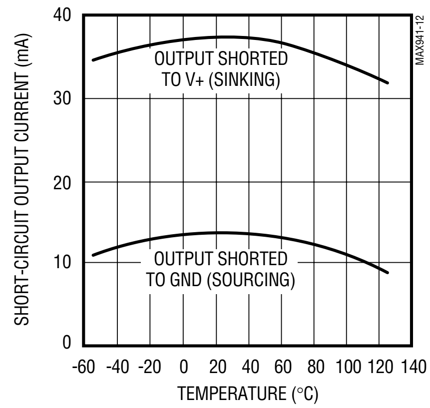
MAX944 TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



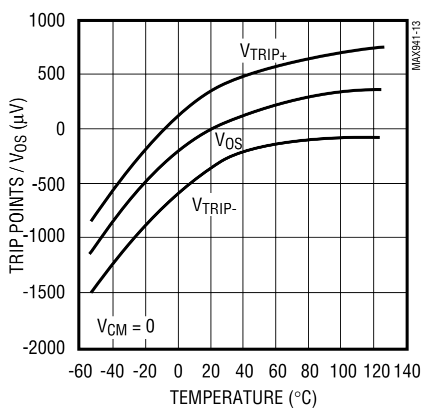
INPUT VOLTAGE RANGE vs. TEMPERATURE



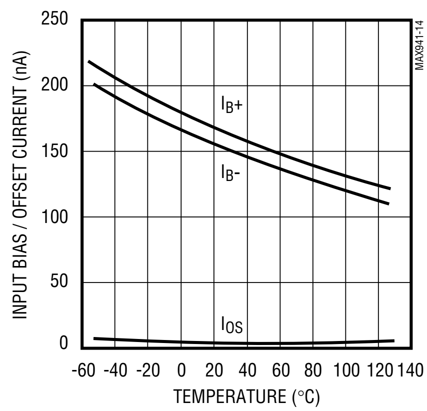
SHORT-CIRCUIT OUTPUT CURRENT vs. TEMPERATURE



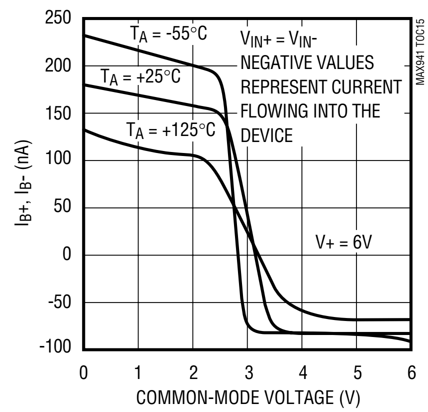
VOLTAGE TRIP POINTS/INPUT OFFSET VOLTAGE vs. TEMPERATURE



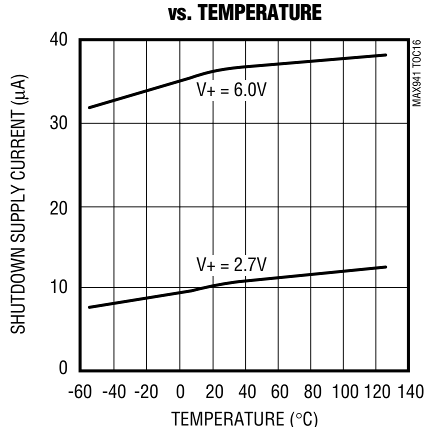
INPUT BIAS CURRENT/INPUT OFFSET CURRENT vs. TEMPERATURE



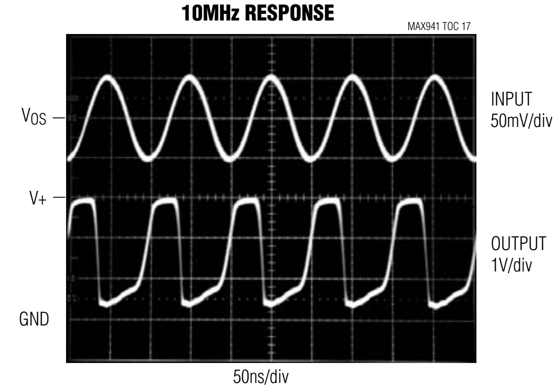
INPUT BIAS CURRENT (I_B+, I_B-) vs. COMMON-MODE VOLTAGE



MAX941 SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



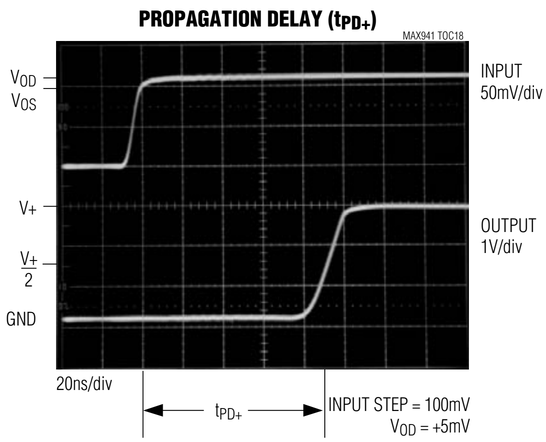
10MHz RESPONSE

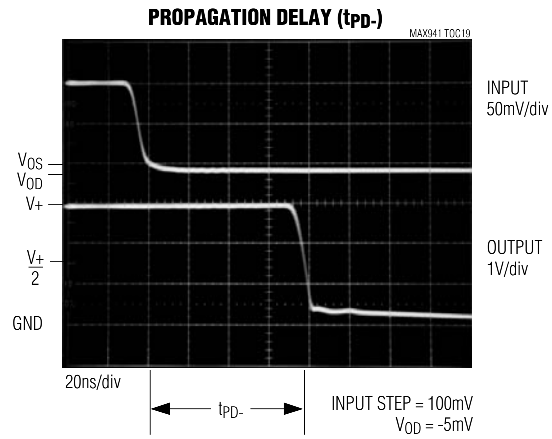


High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

Typical Operating Characteristics (continued)

(V+ = 3.0V, T_A = +25°C, unless otherwise noted.)





Pin Description

PIN			NAME	FUNCTION
MAX941	MAX942	MAX944		
—	1	1	OUTA	Comparator A Output
—	2	2	INA-	Comparator A Inverting Input
—	3	3	INA+	Comparator A Noninverting Input
1	8	4	V+	Positive Supply (V+ to GND must be ≤ 6.5V)
—	5	5	INB+	Comparator B Noninverting Input
—	6	6	INB-	Comparator B Inverting Input
—	7	7	OUTB	Comparator B Output
—	—	8	OUTC	Comparator C Output
—	—	9	INC-	Comparator C Inverting Input
—	—	10	INC+	Comparator C Noninverting Input
6	4	11	GND	Ground
—	—	12	IND+	Comparator D Noninverting Input
—	—	13	IND-	Comparator D Inverting Input
—	—	14	OUTD	Comparator D Output
2	—	—	IN+	Noninverting Input
3	—	—	IN-	Inverting Input
4	—	—	$\overline{SHDN}$	Shutdown: MAX941 is active when $\overline{SHDN}$ is driven high; MAX941 is in shutdown when $\overline{SHDN}$ is driven low.
5	—	—	$\overline{LATCH}$	The output is latched when $\overline{LATCH}$ is low. The latch is transparent when $\overline{LATCH}$ is high.
7	—	—	OUT	Comparator Output
8	—	—	N.C.	No Connection. Not internally connected.

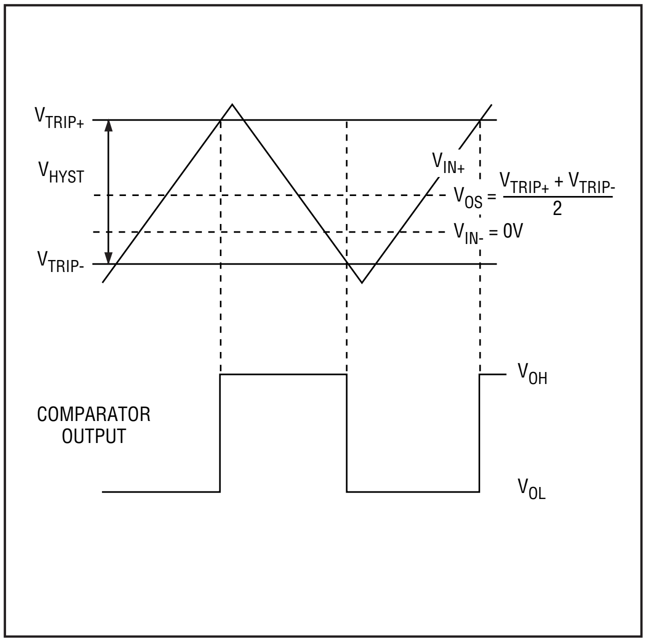


Figure 1. Input and Output Waveform, Noninverting Input Varied

Detailed Description

The MAX941/MAX942/MAX944 single-supply comparators feature internal hysteresis, high speed, and low power. Their outputs are guaranteed to pull within 0.4V of either supply rail without external pullup or pulldown circuitry. Rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment. The MAX941/MAX942/MAX944 interface directly to CMOS and TTL logic.

Timing

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the MAX941/MAX942/MAX944 have internal hysteresis.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The MAX941/MAX942/MAX944's fixed internal hysteresis eliminates these resistors and the equations needed to determine appropriate values.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

The MAX941 includes an internal latch that allows storage of comparison results. The $\overline{\text{LATCH}}$ pin has a high input impedance. If $\overline{\text{LATCH}}$ is high, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is stored when $\overline{\text{LATCH}}$ is pulled low. All timing constraints must be met when using the latch function (Figure 2).

Shutdown Mode (MAX941 Only)

The MAX941 shuts down when $\overline{\text{SHDN}}$ is low. When shut down, the supply current drops to less than 60µA, and the three-state output becomes high impedance. The $\overline{\text{SHDN}}$ pin has a high input impedance. Connect $\overline{\text{SHDN}}$ to V+ for normal operation. Exit shutdown with $\overline{\text{LATCH}}$ high; otherwise, the output will be indeterminate.

Input Stage Circuitry

The MAX941/MAX942/MAX944 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two back-to-back diodes between IN+ and IN- as well as two 4.1kΩ resistors (Figure 3). The diodes limit the differential voltage applied to the internal circuitry of the comparators to be no more than $2V_F$, where V_F is the forward voltage drop of the diode (about 0.7V at +25°C).

For a large differential input voltage (exceeding $2V_F$), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{Input Current} = \frac{(IN+ - IN-) - 2V_F}{2 \times 4.1k\Omega}$$

Input current with large differential input voltages should not be confused with input bias current (I_B). As long as the differential input voltage is less than $2V_F$, this input current is equal to I_B. The protection circuitry also allows for the input common-mode range of the MAX941/MAX942/MAX944 to extend beyond both power-supply rails. The output is in the correct logic state if one or both inputs are within the common-mode range.

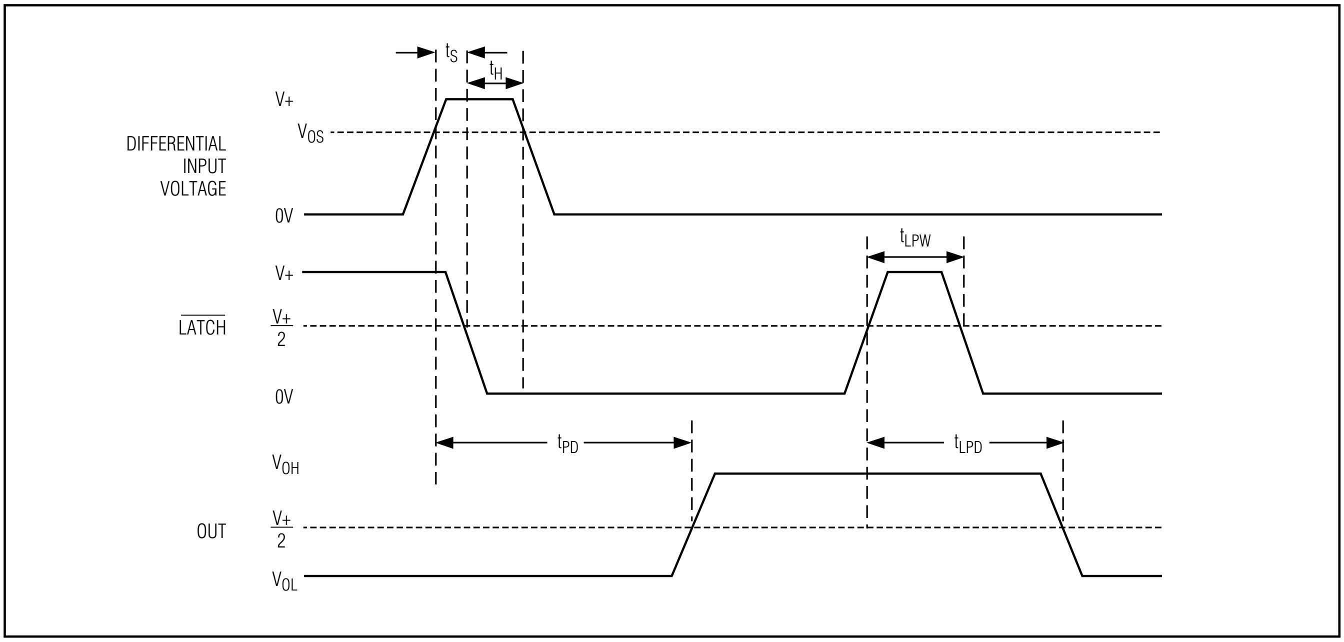


Figure 2. MAX941 Timing Diagram with Latch Operator

Output Stage Circuitry

The MAX941/MAX942/MAX944 contain a current-driven output stage as shown in Figure 4. During an output transition, I_{SOURCE} or I_{SINK} is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches V_{OH} or V_{OL}, the source or sink current decreases to a small value, capable of maintaining the V_{OH} or V_{OL} static condition. This significant decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load will slow down a voltage output transition. This can be useful in noise-sensitive applications where fast edges may cause interference.

Applications Information

Circuit Layout and Bypassing

The high gain bandwidth of the MAX941/MAX942/MAX944 requires design precautions to realize the comparators' full high-speed capability. The recommended precautions are:

1) Use a printed circuit board with a good, unbroken, low-inductance ground plane.
2) Place a decoupling capacitor (a 0.1µF ceramic capacitor is a good choice) as close to V+ as possible.
3) Pay close attention to the decoupling capacitor's bandwidth, keeping leads short.
4) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators.
5) Solder the device directly to the printed circuit board instead of using a socket.

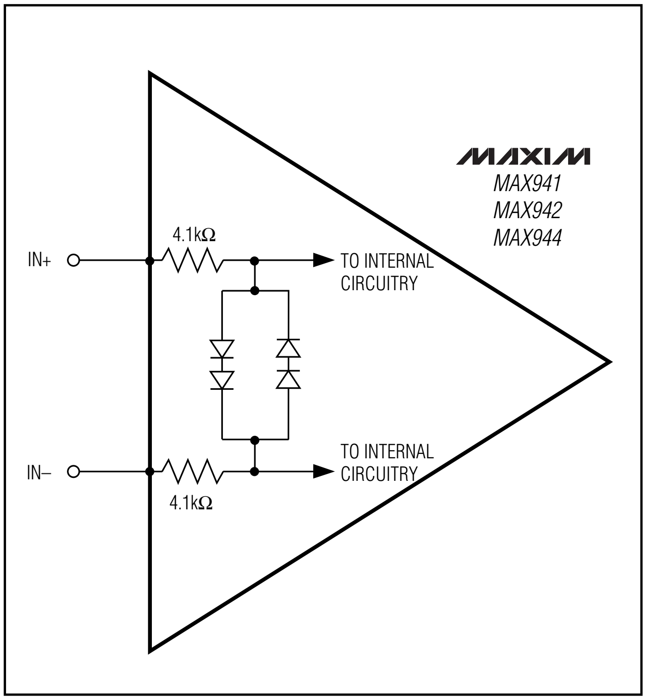


Figure 3. Input Stage Circuitry

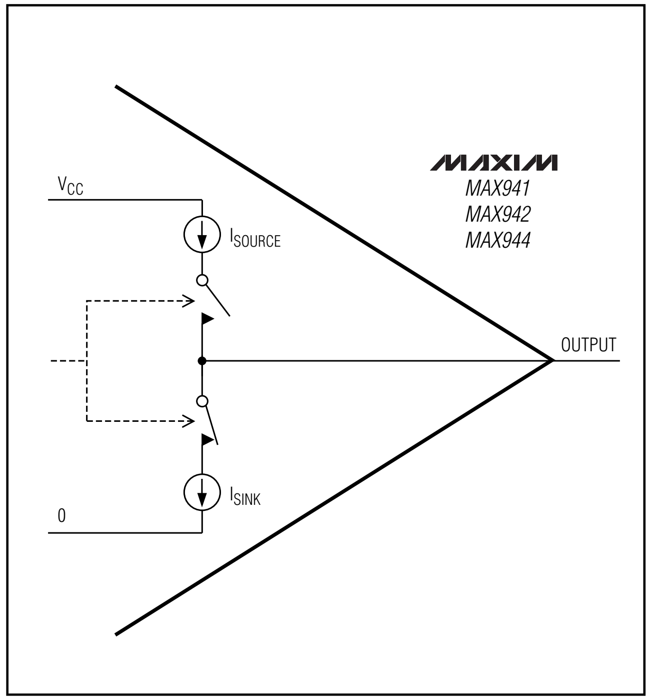


Figure 4. Output Stage Circuitry

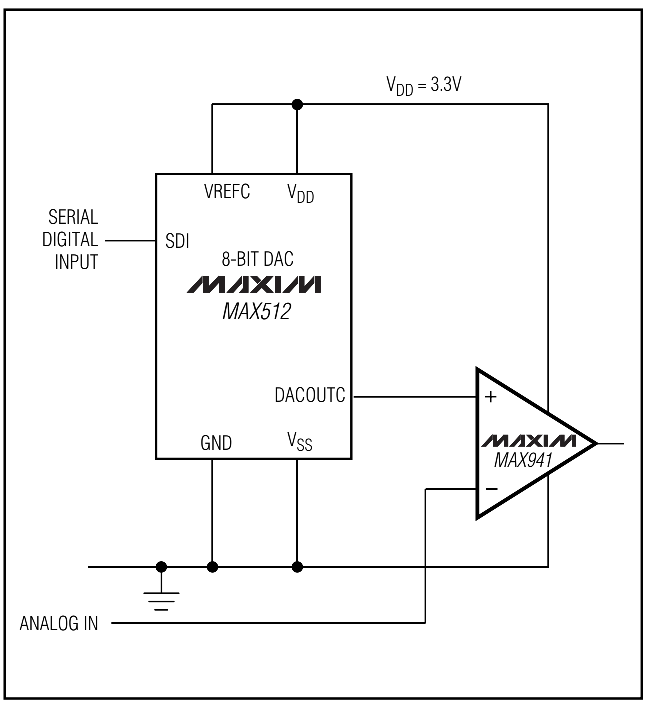


Figure 5. 3.3V Digitally Controlled Threshold Detector

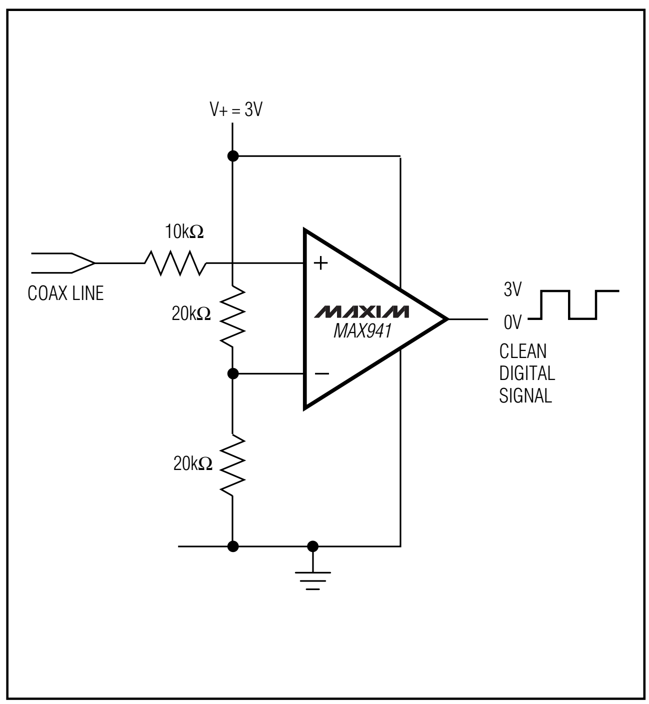


Figure 6. Line Transceiver Application

High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX942MSA/PR*	-55°C to +125°C	8 SO	S8-2
MAX942CPA	0°C to +70°C	8 Plastic DIP	P8-1
MAX942CSA	0°C to +70°C	8 SO	S8-2
MAX942EPA	-40°C to +85°C	8 Plastic DIP	P8-1
MAX942ESA	-40°C to +85°C	8 SO	S8-2
MAX942EUA-T	-40°C to +85°C	8 µMAX-8	U8-1
MAX942AUA-T	-40°C to +125°C	8 µMAX-8	U8-1
MAX944CPD	0°C to +70°C	14 Plastic DIP	P14-3
MAX944CSD	0°C to +70°C	14 SO	S14-1
MAX944EPD	-40°C to +85°C	14 Plastic DIP	P14-3
MAX942ESD	-40°C to +85°C	14 SO	S14-1

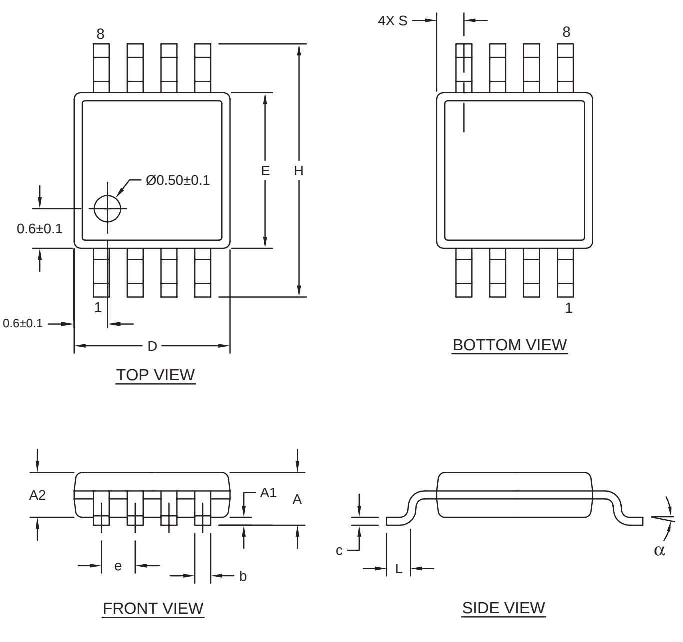
Go to www.maxim-ic.com/PR-1 for details on high-reliability plastic processing.

Chip Information

MAX941 TRANSISTOR COUNT: 192
MAX942 TRANSISTOR COUNT: 314
MAX944 TRANSISTOR COUNT: 620
PROCESS: BiPolar

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



8LUMAXD.EPS

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	

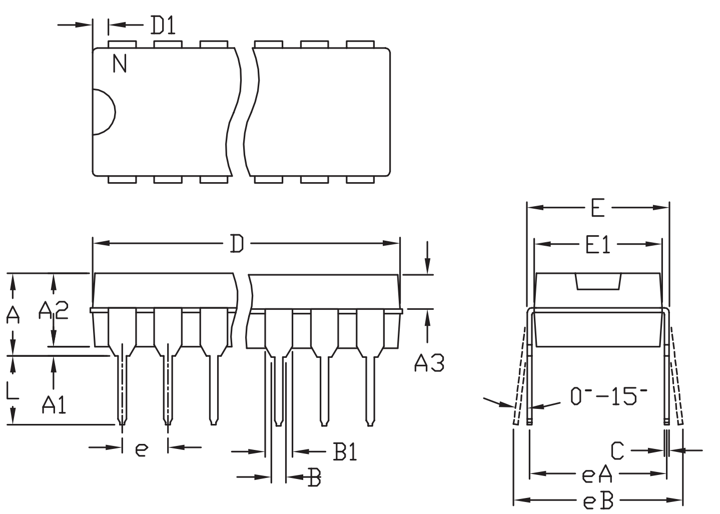
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 8L uMAX/uSOP
APPROVAL | DOCUMENT CONTROL NO. 21-0036 | REV. J | 1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

PDIPN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | DOCUMENT CONTROL NUMBER: 21-0043 REV: D

Revision History

Pages changed at Rev 7: 1, 2, 7–11

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